Final Report on Contract "A Very Large Scale Integrated (VLSI) Circuit Chip Layout for a Low Resolution Accumulator Chip"

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I. Introduction

The layout of a 3-μm CMOS VLSI custom-designed chip of the low resolution accumulator is now reported. This chip is based on the architecture and logic design reported in Dec. 1984. The CIF and CAESAR files for this chip and corresponding cells are deliverable on a magnetic tape. Some test chips are also ready for testing. Since the whole chip contains four pipeline processors, it is nature to test each processor individually. Hence four test chips are designed, each containing a seperate pipeline processor.

All layouts of these chips utilize standard cells. Some JPL CMOS standard cells are modified in order to avoid design rule errors when the cells are inked togther. The design rule check of cells and chips is now finished and verified. The circuit extractor, MEXTRA, is used to obtain the SIM files from CIF files. These extracted circuits are then simulated and verfied by ESIM. The whole chip contains about 7000 transistors and its area is about 288.5 mil x 394.5 mil.

II. About the Chip

The delivered magnetic tape contains two types of files. The CAESAR files are attached by a ".ca" extension on its name and the CIF files are attached by a ".cif" extension. The file name symbolizes the layout. The layout of the low resolution accumulator is named by "chip". Four test chips are named, "chipa", "chipb", "chipc", and "chipd", respectively. The whole layout can be seperated into four distinct parts wherein each part represents almost one pipeline processor. These four parts are named, "parta", "partb", "partc", and "partd", respectively. When these parts are linked togther, a new name "abcd" is given. That is, "abcd" is the layout of "chip" but without pads.

All CIF files are expressed with labels except for those of the chips. The labels are attached mainly for the purpose of simulation. The "chip" contains 33 pads, eight for input data bus, two for the multiplicant (-1, 0, or 1), one for ACC, four for SCALE, one for ROUND, one for LIMIT, two for clocks, one for OVERFLOW FLAG, two for SELECT, one for RDY, eight for output data bus and two for VDD and GND. Hence when it is packaged, it is suggested that a forty pin frame to be used.

A two-phase clock is used. This layout design of the low resolution accumulator satisfies all the specifics of the architecture declared in the report of Dec. 1984. Because the circuit is so large, it is impossible to accomplish the SPICE timing analysis. As aconsequence the working frequency of this accumulator is still unknown. Perhaps the best way to find this data is by direct measurement after this chip is manufactured. Within four pipeline processors, "partc" may be the slowest. But to determine this measurement data is needed.

The whole layout is designed by CMOS standard cells. The JPL CMOS15 standard cells have some design rule checking problems when distinct standard

cells are linked togther. Hence those cells are modified to suit the design rule check. Also, three new standard cells are built, "equi" is an equivalence gate, "trgate" is a transmission gate and "regc" is a static register cell. They appear many times within the chip.

III. The Layout

The attached layout is developed by using the 3-μm CMOS-pw single layer metal technology. The color used on the layout is red for polysilicon, green for diffusion (active), blue for metal, yellow for p-well, brown for p-plus, black for cut and violet for glass. The design rule check of all cells has been finished and verfied by LYRA. It is now ready to be manufactured. Finally, the "abcd" contains 6686 transistors and its area is about 186.6 mil x 294.7 mil. The area of the "chip" is about 288.5 mil x 394.5 mil.

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9280-0180
FOR USE ON HEWLETT-PACKARD RECORDERS

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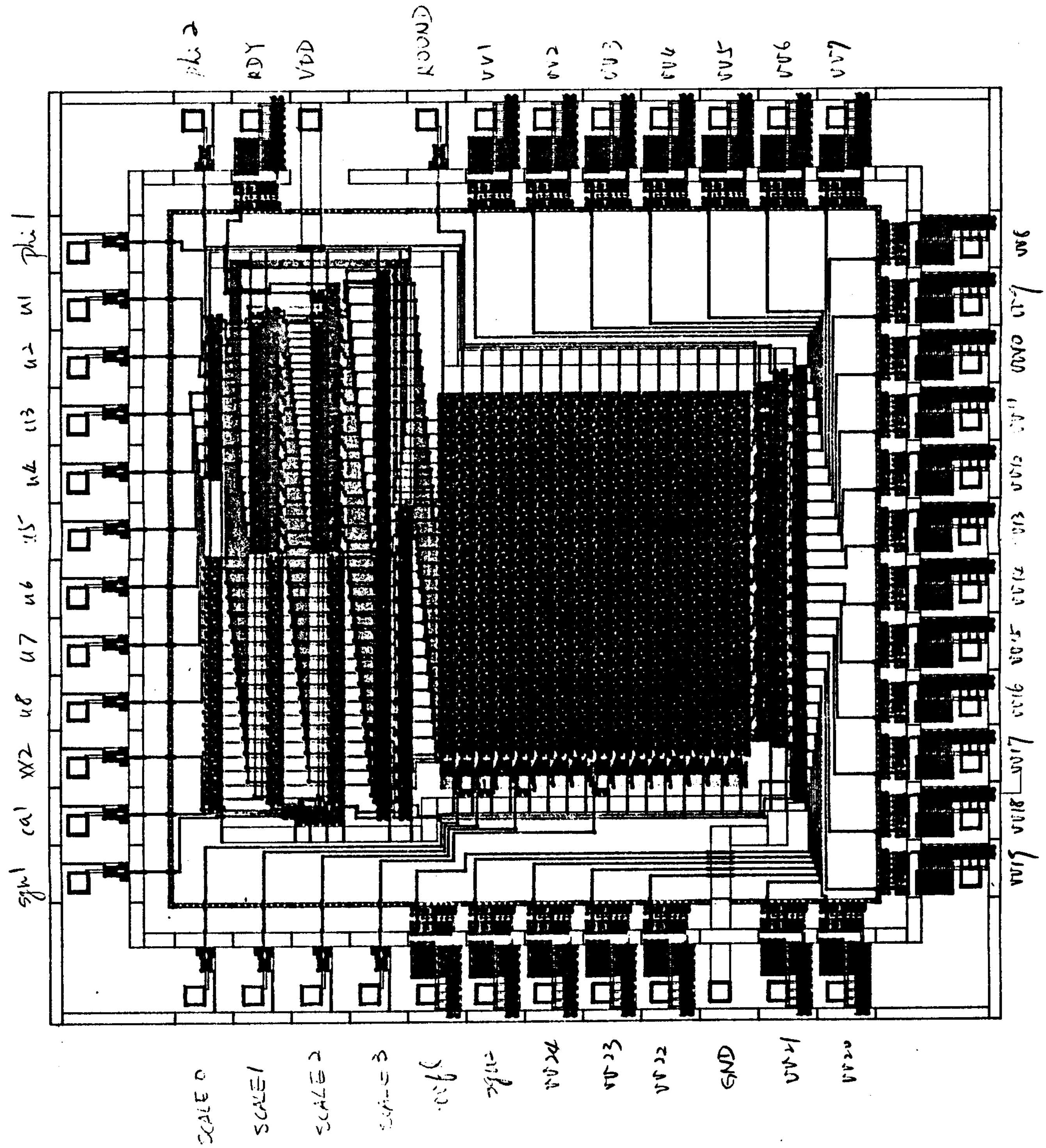
chip c



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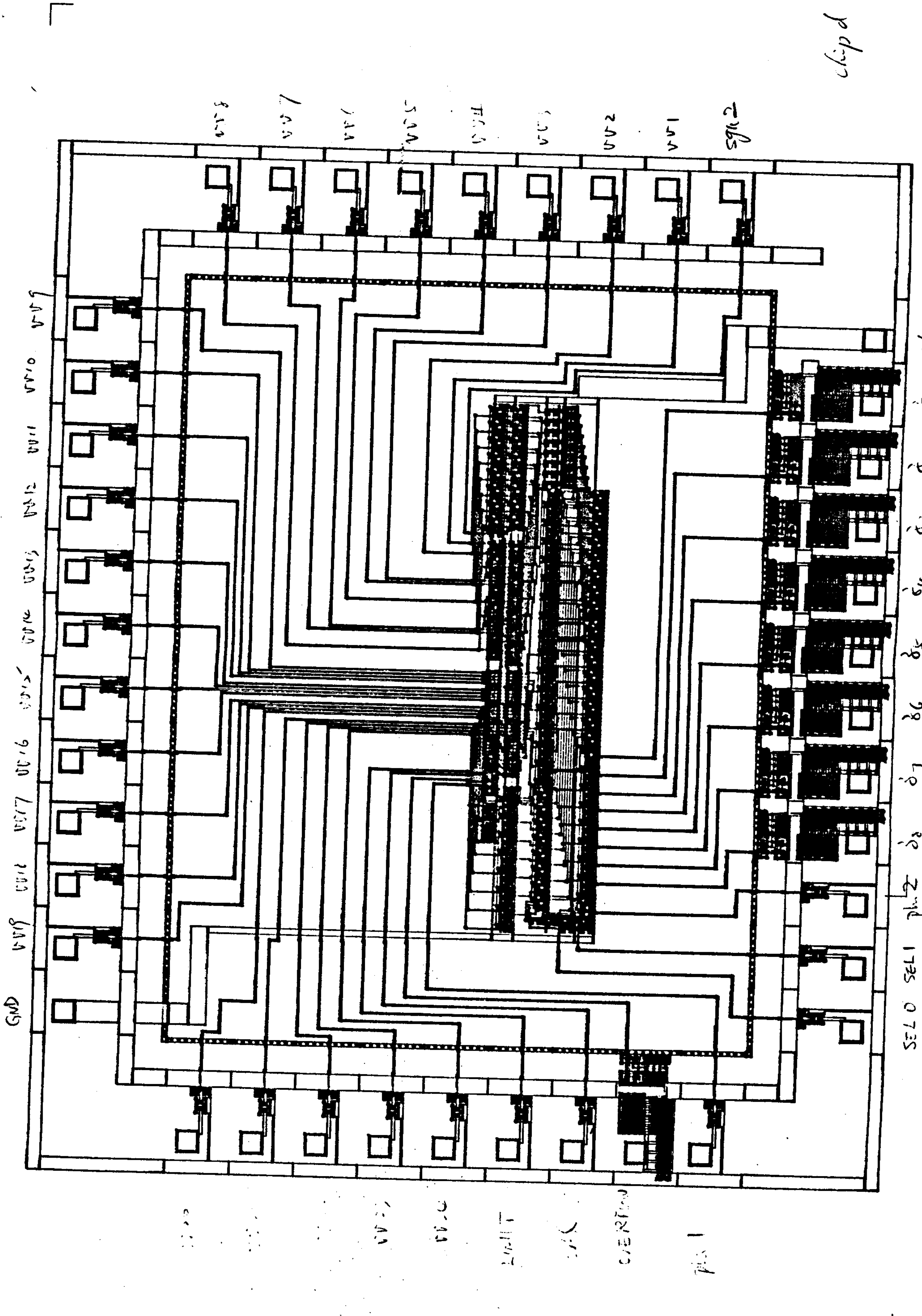

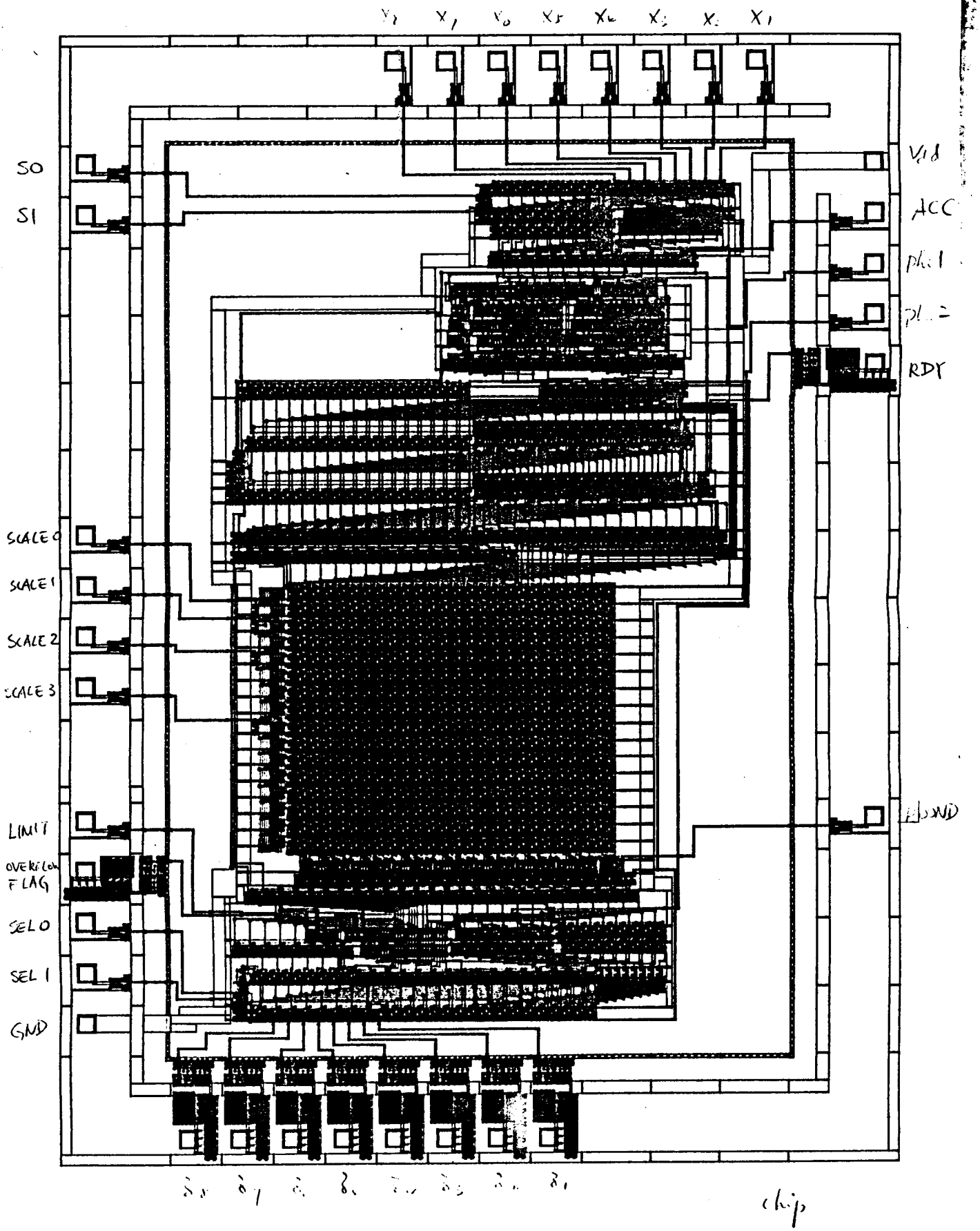

chip